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WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

| EXAMINER | |
|---|---|
| VOCKRODT, JEFF B | |
| **ART UNIT** | **PAPER NUMBER** |
| 2822 | |

DATE MAILED: 06/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/919,797 | KUBO, HIROTOSHI | |
| | Examin r | Art Unit | |
| | Jeff Vockrodt | 2822 | |

*-- The MAILING DATE of this communication appears on the cov r she t with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3,4 and 6-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 6-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

This office action is in response to the amendment filed on May 20, 2003. Claims 1, 3-4, and 6-8 are pending.

### *Claim Interpretation*

"[D]uring examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification." In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000) (citing In re Graves, 69 F.3d 1147,1152, 36 USPQ2d 1697,1701 (Fed. Cir. 1995); In re Etter, 756 F.2d 852, 858, 225 USPQ 1, 5 (Fed. Cir. 1985) (en banc)). "The PTO broadly interprets claims during examination of a patent application since the applicant may 'amend his claim to obtain protection commensurate with his actual contribution to the art.'" In re Yamamoto, 740 F.2d 1569, 1571, 222 USPQ2d 934, 936 (Fed Cir. 1984) (quoting In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550 (CCPA 1969)). "[T]he name of the game is the claim." In re Hiniker Co., 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

1. A method of manufacturing a semiconductor device, comprising:
forming a collector layer of a first conductivity type;
forming a base region of a second conductivity type formed on a top surface of said collector layer of said first conductivity type, said first conductivity type being opposite said second conductivity type, said base region being formed using epitaxial growth technology, and being formed as a single region having a uniform depth;
forming a groove in a top surface of said base region at a portion thereof;
forming spacers on sidewalls of said groove;
forming a diffusion source film in said bottom surface of said groove to be embedded therein between said spacers; and
forming an emitter region of said first conductivity type in said base region at a bottom surface of said groove, said emitter region being formed in said top surface of said base region at a bottom of said diffusion source film between said spacers. (examiner's emphasis)

Does the order of steps recited in claim 1 exclude growing an epitaxial layer for the base and then doping the base? First, it is noted that the top surface of the collector region (11) is defined by the depth of the base doping layer (13) (see Fig. 5B). The specification teaches that

the invention may include the sequence of (1) growing an epitaxial layer and (2) doping by thermally diffusing dopants:

> [0018] The base region 13 comprises either a diffusion region formed by thermal diffusion at a prescribed diffusion depth or a semiconductor layer formed on the surface of the layer 11 by vapor deposition and having a uniform distribution of impurity concentration in the vertical direction of the layer.

Thus, if the claim is interpreted to exclude forming a base region using epitaxy followed by diffusing dopants to form the base layer then one of the disclosed embodiments would not fall within the scope of claim 1. "As a general rule, claim interpretations, which operate to exclude the preferred embodiment, are 'rarely, if ever, correct and require highly persuasive evidentiary support.'" Lacks Industries Inc. v. McKechnie Vehicle Components USA Inc., 66 USPQ2d 1083 (Fed. Cir. 2003) (quoting Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1583, 39 USPQ2d 1573, 1578 (Fed. Cir. 1996)). Moreover, claim 3, which depends from claim 1, requires forming the base region by a diffusion of impurities at a prescribed diffusion depth. Indeed, the subject matter of claim 3 must fall within the scope of claim 1 for claim 3 to be valid under 35 U.S.C. § 112. Accordingly, claim 1 permits the base to be formed by epitaxial growth technology followed by doping the base.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 1, 3-4, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 4,997,775 ("Cook").**

Cook teaches a method of forming a bipolar transistor. A collector region (16) is formed using epitaxy; a base region (66, 68) is formed in a portion of the epitaxial region (16) by dopant diffusion and ion implantation (Fig. 6), thereby forming a base region (66, 68) on the top surface of the collector region (16); sidewall spacers (66B) are formed on the sidewall (28A) of grooves in the base region (66, 68) (Fig. 7); a diffusion source (71) is formed between the spacers; and an emitter (74) is formed by outdiffusion from the diffusion source (Fig. 8).

**Claim 1 reads on Cook as follows:** A method of manufacturing a semiconductor device, comprising:

forming a collector layer (N- region 16; Fig. 6) of a first conductivity type;

forming a base region (P region 66 and P+ region 68; Fig. 6) of a second conductivity type formed on a top surface of said collector layer of said first conductivity type, said first conductivity type being opposite said second conductivity type, said base region being formed using epitaxial growth technology (the p-type base diffusion is formed in an epitaxial layer 16), and being formed as a single region having a uniform depth (66, 68 form a single region of uniform depth[1]);

forming a groove (62; Fig. 6) in a top surface of said base region at a portion thereof;

forming spacers (66B) on sidewalls (28A) of said groove (62);

forming a diffusion source film (71, Fig. 8) in said bottom surface of said groove (62) to be embedded therein between said spacers (66B); and

forming an emitter region (N+ region 74) of said first conductivity type in said base region (66, 68) at a bottom surface of said groove, said emitter region (74) being formed in said top surface of said base region (66, 68) at a bottom of said diffusion source film (71) between said spacers (66B).

Claim 3. A method of manufacturing a semiconductor device according to claim 1, wherein said base region (66, 68) is formed on said top surface of said collector layer (66, 68) by a diffusion of impurities at a prescribed diffusion depth (col. 5, ll. 9-24).

Claim 4. A method of manufacturing a semiconductor device according to claim 1, wherein said base region (66, 68) has a flat bottom surface beneath said emitter region (74) and beneath a base electrode (52D; Fig. 8)).

Claim 8. A method of manufacturing a semiconductor device according to claim 1, wherein said diffusion source film (71) is a polycrystalline silicon layer having impurities for emitter diffusion (74) (col. 5, ll. 45-51).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cook in view of U.S. Pat. No. 4,731,341 ("Kawakatsu").**

Claims 6-7 depend from claim 1 which is addressed above. Claim 6 differs from Cook by forming an emitter electrode on the surface of the diffusion source film. Claim 7 differs from Cook by forming the base and emitter electrodes of aluminum. Cook merely teaches a doped polysilicon diffusion source film (71) that serves as the emitter electrode.

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[1] This is in contrast to applicant's prior art Fig. 1, which shows base regions 3, 8 having a non-uniform depth.

Kawakatsu teaches forming a bipolar transistor utilizing an arsenic doped polysilicon emitter contact layer 116 from which the emitter dopants are diffused and an aluminum emitter electrode 116. (Kawakatsu, col. 4, ll. 50-60).

Cook and Kawakatsu are analogous art. They are within the field of bipolar transistors and particularly teach forming diffused emitters.

Further forming an aluminum electrode onto the emitter electrode (71) of Cook would have been obvious to one of ordinary skill in the art at the time of the invention. A person having ordinary skill in the art would have been motivated to form an aluminum electrode in addition to the emitter electrode of Cook to facilitate improved electrical contact to the emitter as suggested by Kawakatsu.

***Response to Arguments***

Applicant's arguments filed 5-20-03 ("Reply") have been fully considered but they are not persuasive.

Applicant's first argument is that forming a base region "using epitaxial growth technology" reduces the variation in width of the base region compared to conventional technology such as thermal diffusion and ion implantation. In response, anticipation does not require that a reference "teach" what appellant teaches, but only that the claims "read on" something disclosed in the reference. Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 722, 218 USPQ 781, 789 (Fed. Cir. 1983). At any rate, applicant's statement is overbroad since epitaxial growth technology only concerns doping in the limited instance where the dopant is added during the epitaxial process (i.e., in-situ doping). The examiner understands the disclosed in-situ doping during epitaxial growth of the base layer to be a more precise cause of the reduction in non-uniformity and one that is not shown in the references of record. Currently, none of the claims reflect this distinction.

Applicant asserts that "the Cook reference merely teaches forming a base region in the conventional manner discussed in this application." (Reply, page 3.) This is clearly wrong as a matter of fact. Nowhere in the present application is it admitted that the prior art uses any form of epitaxy whatsoever, yet Cook teaches forming epitaxial base and collector layers. Additionally, Cook establishes that applicants were not the first to form a base in a single region (i.e., free of a graft structure). Cook therefore shows at least two claimed features that are not reflected in applicant's originally filed view of the prior art as represented by Fig. 1 of this application. Therefore, the examiner does not understand why applicant views Cook as "merely teach[ing] forming a base region in the conventional manner discussed in this application." The rejections stand as originally set forth in the office action mailed November 20, 2002.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (703) 306-9144 who can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (703) 308-4905.

The fax numbers for this Group are (703) 305-3432, (703) 308-7722, (703) 305-3431, and (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

June 19, 2003
J. Vockrodt

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800